

SEMICONDUCTOR DIFFERENTIAL INTERCONNECT

TECHNICAL FIELD

[0001] The present invention generally relates to the field of electronic devices and particularly to an interconnect in a semiconductor device.

BACKGROUND

[0002] MicroElectroMechanical Systems (MEMS) are a class of devices that integrate small mechanical and electrical components. A single MEMS device may measure from several nanometers to a few microns, with an array of MEMS devices provided within a few millimeters.

[0003] MEMS may be integrated with electronic circuitry. For example, a MEMS device may be incorporated with an integrated circuit (IC) to provide expanded functionality, such as microelectric actuators incorporated with electronic circuitry, e.g. an airbag sensor.

[0004] To communicatively couple MEMS devices, both between the MEMS devices themselves and with other electronic devices, signals are transmitted between devices. Signals may be transmitted for a variety of purposes, such as for timing, activation, data transfer, and the like.

[0005] Electromagnetic interference may limit the ability of a MEMS device to provide desired functionality. For instance, electromagnetic interference (EMI) may limit a signal that is transmitted by an interconnect between devices. The EMI may originate both from outside a system employing a MEMS device as well as within the system itself. To compensate for the EMI, devices may operate at reduced system speeds to enable effective signal passage, provide an interconnect of increased distance between devices to limit exposure of the EMI between the devices, and the like.

[0006] To increase signal integrity in a MEMS system, an interconnect that uses differential signaling may be employed. However, previous interconnect structures that provided differential signaling did not preserve the differential signaling with integrity when EMI was encountered. As such, the EMI was incorporated into the differential signaling that was transmitted through the

interconnect, thereby decreasing the signal-to-noise ratio of the differential signaling.

[0007] Therefore, it would be an advance in the art to provide an interconnect which preserves differential signal integrity.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The same components are used throughout the drawings to reference like features and components.

[0009] FIG. 1 is an illustration of an exemplary embodiment of the present invention in which a cross-sectional view of an interconnect is shown.

[0010] FIG. 2 is a circuit diagram of an exemplary embodiment of the present invention in which capacitance of an interconnect is shown.

[0011] FIG. 3 is an illustration of an exemplary embodiment of the present invention in which symmetry of an interconnect is shown.

[0012] FIG. 4 is an illustration of an exemplary embodiment of the present invention in which asymmetric surface areas of first and second conductors is compensated for by positioning of the first and second conductors to provide substantially equivalent amounts of EMI to the first and second conductors.

[0013] FIG. 5 is an illustration of an exemplary embodiment of the present invention in which an interconnect with D-shaped conductors is shown.

[0014] FIG. 6 is an illustration of an exemplary embodiment of the present invention in which an interconnect with rectangular-shaped conductors is shown.

[0015] FIG. 7 is an illustration of an exemplary embodiment of the present invention in which a semiconductor device employing an interconnect is shown.

[0016] FIG. 8 is a flow diagram depicting an exemplary embodiment of the present invention in which encountered electromagnetic interference is distributed and removed from a transmitted signal.

[0017] FIG. 9 is a flow diagram depicting an exemplary embodiment of the present invention in which an interconnect is formed.

[0018] FIG. 10 is an illustration of an exemplary embodiment of the present invention in which conductors of an interconnect are formed from a semiconductor substrate.

[0019] FIG. 11 is a further illustration of the exemplary embodiment of the present invention as depicted in FIG. 10 and in which an insulator is formed which substantially surrounds the conductors of the interconnect.

[0020] FIG. 12 is an illustration of an exemplary embodiment of the present invention in which openings in an insulator are filled, where the openings were formed when the insulator was grown.

DETAILED DESCRIPTION

[0021] OVERVIEW

[0022] An interconnect with conductors is provided that preserves differential signal integrity. In one embodiment of the present invention, electromagnetic interference (EMI) is symmetrically distributed to conductors of the interconnect whereby the symmetrically distributed EMI may be removed from a differential signal being transmitted through the conductors of the interconnect.

[0023] In another embodiment of the present invention, an interconnect includes a first conductor and a second conductor. The first and second conductors each transmit a different portion of a differential signal. The interconnect includes a third conductor that distributes EMI encountered by the third conductor to the first conductor and the second conductor to preserve the integrity of the differential signal in the first and second conductors. The third conductor can be arranged such that the first conductor and the second conductor are exposed to substantially equivalent amounts of EMI. The EMI may then be removed from the differential signal, thereby preserving differential signal integrity.

[0024] FIGS. 1 through 12 illustrate exemplary embodiments of an interconnect of the present invention. Each interconnect in each embodiment of the present invention may be used in a variety of electronic device applications, such as in a MicroElectroMechanical system (MEMS). Although the following discussion will describe an interconnect in a MEMS application, a variety of applications are contemplated, such as electronic device applications including memories,

semiconductor devices, application specific integrated circuits (ASIC), and the like.

[0025] A MEMS device having an interconnect may be constructed so as to be integral with a semiconductor substrate, such as a silicon wafer, polysilicon, glass, and the like, where features of the MEMS device are provided on the semiconductor substrate utilizing a variety of techniques. For example, the fabrication of the interconnect may include deposition, etching, photolithography, micromachining, and other semiconductor fabrication processes.

[0026] The semiconductor substrate may transmit EMI from switching circuits, power circuits, and the like which may affect signal transmission. The EMI may degrade signals transmitted through the semiconductor substrate. To increase signal integrity, differential signaling in an interconnect may be employed. Differential signals may be provided through a pair of conductors in the interconnect which are utilized as a reference, one to the other. Because the differential signals transmitted on the conductors are utilized to reference each other, EMI may be removed from the differential signals that are transmitted on the conductors.

[0027] For instance, a first conductor in an interconnect may be utilized to carry a first portion of the differential signal, while the second conductor in the interconnect carries a second portion of the differential signal that is equal and opposite to the signal carried on the first conductor (i.e., such as opposite polarity). EMI, which is common between the first conductor and the second conductor, may be subtracted from the differential signal in what may be referred to as common mode rejection, to provide an output signal from the interconnect which is free from the encountered EMI.

[0028] In another embodiment of the present invention, a first conductor and a second conductor in an interconnect are utilized to indicate a logical state. Substantially equivalent amounts of EMI are applied to the first and second conductors of the interconnect. The first conductor has a first portion of a differential signal that is higher than a second portion of the differential signal on the second conductor. The difference between these signals indicates a first logical state. If the first conductor has a first portion of a differential signal that is

lower than a second portion of the differential signal on the second conductor, a second logical stage is indicated. By referencing the first portion to the second portion, EMI may be removed from the differential signal.

EXEMPLARY EMBODIMENTS OF THE PRESENT INVENTION

[0029] FIG. 1 is a cross-sectional view taken perpendicular to a longitudinal axis of an interconnect 100 that extends into and out of the page. The interconnect 100 is disposed within a semiconductor substrate 102. The term "semiconductor substrate", as used herein, includes semiconductive material. The term is not limited to bulk semiconductive material, such as a silicon wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. A semiconductor substrate may be made of silicon, polysilicon, gallium arsenide, silicon on sapphire (SOS), epitaxial formations, germanium, germanium silicon, diamond, silicon on insulator (SOI) material, selective implantation of oxygen (SIMOX) substrates, and the like substrate materials. In embodiments of the present invention, the semiconductor substrate 102 is made of silicon, which can be a monocrystalline silicon wafer.

[0030] The interconnect 100 includes a first conductor 104 and a second conductor 106. The first conductor 104 and a second conductor 106 provide conductive paths for transmitting signals. The first conductor 104 is proximal to the second conductor 106. A variety of signals may be respectively transmitted by the first conductor 104 and the second conductor 106. For example, the first conductor 104 may transmit a first portion of a differential signal and the second conductor 106 may transmit a second portion of the differential signal. The portions of the differential signal are used as a reference one to the other so that EMI can be removed.

[0031] A first insulator 108 is included in the interconnect 100 to electrically insulate the first conductor 104 from the second conductor 106. The first insulator 108 may be formed from a range of electrically-insulating materials, such as dielectric materials and the like. A dielectric material is a substance that is a poor conductor of electricity, but efficiently supports electrostatic fields. Dielectric materials may include porcelain (ceramic), mica, glass, plastics, oxides

of various metals, and the like. Liquids and gases may also serve as dielectric materials, such as dry air and distilled water, as well as a vacuum.

[0032] The interconnect 100 includes a third conductor 110 which substantially surrounds each of the first conductor 104, the second conductor 106, and the first insulator 108. In the Figures, the first conductor 104 is also referenced as C1, the second conductor 106 is referenced as C2, and the third conductor is referenced as C3. The first insulator 108 electrically insulates the third conductor 110 from both the first conductor 104 and the second conductor 106. A second insulator 112, which substantially surrounds the third conductor 110, electrically insulates the third conductor 110 from the semiconductor substrate 102.

[0033] The third conductor 110 can be formed so as to act as a shield to the first and second conductors 104, 106. For example, the third conductor 110 may shield at least a portion of the EMI that it encounters from affecting the first conductor 104 and the second conductor 106. This shielding function may include reflecting EMI, absorbing EMI, and the like.

[0034] An amount of EMI may be encountered which is greater than the third conductor 110 is capable of shielding. Here, the third conductor 110 can be formed so as to provide substantially equivalent distributions of EMI to the first and second conductors 104, 106. As such, this equivalent distribution of EMI by the third conductor 110 preserves the integrity of any differential signal that is transmitted through the interconnect 100 via the first and second conductors 104, 106. By providing a substantially equivalent distribution, the EMI can be incorporated within any portion of any differential signal that is respectively transmitted through the first and second conductors 104, 106 so as to be substantially equivalent in both amount and manner. EMI, which is common to both the first conductor 104 and the second conductor 106, may be removed by referencing the signals received from the first conductor and the second conductor 106 to each other, such as through common mode rejection. Thus, because substantially equivalent distributions of EMI were included within the portions of the differential signals, a substantial amount of the EMI may be removed, thereby preserving the integrity of the differential signal.

[0035] The interconnect 100 may be formed so as to include several capacitors. For instance, one capacitor can be formed by the third conductor 110 being separated from the semiconductor substrate 102 by the second insulator 112. Likewise, the third conductor 110 may act as a capacitor in combination with the first conductor 104 and the first insulator 108, and in combination with the second conductor 106 and the first insulator 108.

[0036] FIG. 2 is a circuit diagram illustrating the interconnect 100 of FIG. 1. A first capacitor 202 ($\text{Cap}_{\text{substrate}/C_3}$) is formed from the semiconductor substrate 102, the second insulator 112, and the third conductor 110. A second capacitor 204 (Cap_{C_1/C_3}) is formed from the third conductor 110, the first insulator 108, and the first conductor 104. Likewise, a third capacitor 206 (Cap_{C_2/C_3}) is formed from the third conductor 110, the first insulator 108, and the second conductor 106.

[0037] The first capacitor 202 couples EMI from the semiconductor substrate 102 to the third conductor 110. The third conductor 110 symmetrically distributes the EMI using the second capacitor 204 to the first conductor 104, and using the third capacitor 206 to the second conductor 106, respectively. Therefore, a path of EMI to the first conductor 104 from the semiconductor substrate 102 through the third conductor 110 is substantially equivalent to a path of EMI from the semiconductor substrate 102 through the third conductor 110 to the second conductor 106. For example, EMI may be transmitted through the first capacitor 202 to be exposed in substantially equivalent amounts to the first conductor 104 and the second conductor 106 using the second capacitor 204 and the third capacitor 206, respectively.

[0038] Overall capacitance from the first conductor 104 to the semiconductor substrate 102 and from the second conductor 106 to the semiconductor substrate 102 is reduced by the presence of the third conductor 110. Thus, the third conductor 110 acts to shield capacitance from the semiconductor substrate 102. Therefore, lower signal strengths may be used in transmitting signals through interconnect 100. One example is a read back signal from a diode sensor that is transmitted through the interconnect, where the read back signal may involve currents on the order of 200 nA and less. Isolating the read back signal from EMI is desirable to maintain signal to noise ratio (SNR) of a differential signal. By

providing the third conductor 110 as a shield, signal amplitude may be small with respect to EMI encountered from the semiconductor substrate 102.

[0039] FIG. 3 illustrates an embodiment of the present invention wherein symmetry of the interconnect 100 is shown. To provide substantially equivalent amounts of EMI, the interconnect 100 may be symmetrically configured. Symmetrical configuration promotes integrity of the differential signal by exposing corresponding parts of the first conductor 104 and the second conductor 106 to substantially equivalent amounts of EMI .

[0040] In an embodiment of the present invention, the interconnect 100 provides substantially equivalent amounts of EMI through symmetrical positioning of the first conductor 104 and the second conductor 106 with respect to the third conductor 110. The first conductor 104 and the second conductor 106 are separated by equal distances from the third conductor 110. Capacitance is inversely proportional to distance between conductors. Therefore, by providing corresponding segments of the first conductor 104 and the second conductor 106 at the corresponding distance, capacitance between the first conductor 104 and the third conductor 110 is substantially equivalent to capacitance between the second conductor 106 and the third conductor 110. Further, through use of the third conductor 110, capacitance between the semiconductor substrate 102 and the first conductor 104 is substantially equivalent to capacitance between the semiconductor substrate 102 and the second conductor 106.

[0041] In an additional embodiment of the present invention, substantially equivalent amounts of EMI are provided based on configuration of the respective surface areas of the first conductor 104, the second conductor 106, and the third conductor 110. Capacitance is directly proportional to surface areas of the conductors. Therefore, capacitance between the first conductor 104 and the third conductor 110 may be varied based on surface area, such as by varying surface area of one or both of the first conductor 104 and the third conductor 110. Likewise, the surface area of the second conductor 106 may also be varied with respect to the third conductor 110 to vary capacitance. For example, during a manufacturing process, the first conductor 104, the second conductor 106, and the third conductor 110 may be formed to have surfaces areas to increase or

decrease capacitance between the first conductor 104 and the third conductor 110 and the capacitance between the second conductor 106 and the third conductor 110. By increasing or decreasing the capacitance when manufacturing the interconnect 100, substantially equivalent amount of EMI may be transmitted to the first and second conductors 104, 106 during use of the interconnect 100.

[0042] In a further embodiment of the present invention, substantially equivalent amounts of EMI are provided based on insulators used. Capacitance also depends on a dielectric constant of a dielectric separating the conductors of a capacitor, such as the first insulator 108 and second insulator 112. By varying the dielectric constant of parts of the first insulator 108 disposed between the first conductor 104, the second conductor 106 and the third conductor 110, capacitance may be varied as desired. For example, an embodiment may include an insulator 108 having different dielectric constants of a first part 302 of the first insulator 108 disposed between the first conductor 104 and the third conductor 110 as opposed to a second part 304 of the first insulator 108 disposed between the second conductor 106 and the third conductor. Additionally, the second insulator 112, disposed between the third conductor 110 and the semiconductor substrate 102, may have a dielectric constant to produce a variety of results, such as increased shielding, increased transmittance, and the like.

[0043] The interconnect 100 may assume a variety of configurations yet still provide substantially equivalent amounts of EMI. For example, substantially equivalent amounts of EMI may be provided when designing an interconnect through symmetrical shielding and/or distribution of EMI and/or capacitance from the third conductor 110 to the first conductor 104 and the second conductor 106. Additionally, different combinations of factors may be used to achieve a desired result. As shown in the exemplary embodiment of the present invention depicted in FIG. 4, combinations of factors may be used to provide substantially equivalent amounts of EMI. By varying at least two of distance, surface area and materials used in forming an interconnect 400, factors may be used in combination to provide substantially equivalent amounts of EMI. For example, factors such as distance and surface area of a first conductor 402, a second conductor 404 and/or a third conductor 406 of the interconnect 400 may be compensated for by

another factor. The first conductor 402 may be formed with a smaller surface area than the second conductor 404, but is positioned closer to the third conductor 406 than the position of the second conductor 404. Likewise dielectric constants of material may be varied, as described in relation to FIG. 4, between the first, second and third conductors 402, 404, and 406 to compensate for varying distances. Therefore, substantially equivalent amounts of EMI are provided to the third conductor 406 to the first and second conductors 402, 404.

[0044] FIG. 5 illustrates an exemplary embodiment of the present invention wherein an interconnect 500 with a reduced cross-sectional area is shown. To provide a smaller cross-sectional area of the interconnect 500, a first conductor 502 and a second conductor 504 may be formed to have opposing substantially parallel planar sides 506 and 508. The substantially parallel planar sides 506, 508 of the first and second conductors 502, 504 enable closer positioning and therefore results in a smaller cross-sectional area of the interconnect 500.

[0045] The thickness of the first insulator 512 surrounding the first and second conductors 502 and 504 may also be configured to achieve desired results. For example, to achieve a generally uniform thickness of the first insulator 512, the outer surfaces 514 and 516 of the first conductor 502 and the second conductor 504 are formed in a generally elliptical shape. The outer surfaces 514 and 516 are at corresponding distances from the third conductor 518. The third conductor 518 is formed to have a shape which corresponds to a shape of the outer surfaces 514 and 516 of the first and second conductors 502 and 504. Through the combination of the generally elliptical shape of the outer surfaces 514 and 516 and the substantially planar opposing sides 506 and 508 of the first conductor 502 and the second conductor 504, a generally D-shaped structure is provided. This D-shaped structure provides a smaller cross-sectional area of the interconnect 500. The cross-sections depicted in Fig. 5 are taken from a plane perpendicular to a longitudinal axis of each of the first and second conductors 502, 504. Moreover, the first conductor 502, the second conductor 504, and the third conductor 518 may be formed in a variety of shapes, such as a rectangular interconnect 600 shown in the exemplary embodiment of the present invention depicted in FIG. 6, polygonal, rounded, and the like.

[0046] FIG. 7 is an illustration of an exemplary embodiment of the present invention in which a semiconductor device 700 employing an interconnect 702 is shown. The semiconductor device 700, which is shown in phantom, is portion of a MEMS assembly (not shown). The semiconductor device 700 includes a first layer 704, a second layer 706 and a third layer 708 formed from a semiconductor substrate. The second layer 706 is disposed between the first layer 704 and the third layer 708. The first, second and third layers 604, 706 and 708 are formed from a semiconductor substrate. The interconnect 702 can be used to transmit signals between layers 704-708.

[0047] A source device 710, which outputs a differential signal, is disposed in the first layer 704. The source device 710 may include a wide range of electrical devices, MEMS devices, and the like. To transmit a signal from the source device 710 to a receiving device 712, which is shown in phantom, disposed in the third layer 708, the interconnect 702 is provided in the second layer 706. The receiving device 712 may also include a wide range of electrical devices (e.g. a differential signal amplifier), MEMS devices, and the like.

[0048] The source device 710 and the receiving device 712 may be communicatively coupled to the interconnect 702 in a variety of ways. For example, a metallization 714 to the interconnect 702 may be provided to transmit signals from the source device 710 to the interconnect 702, or to transmit signals from the interconnect 702 to the receiving device 712. The metallization 714 can be, for instance, a via, a metal contact, and the like.

[0049] During fabrication of the semiconductor device 700, and prior to the formation of a third conductor 716, a passage may be provided to first and second conductors 718 and 720 so that the metallization 714 may be formed. The third conductor 716 still substantially surrounds the first conductor 718 and the second conductor 720 along a substantial portion of a longitudinal axis of each of the first conductor 718 and the second conductor 720.

[0050] Although the semiconductor device 700 configured as a three-layered structure is shown, the interconnect 702 may be incorporated in layers in a variety of ways. For example, the interconnect 702 may supply a conductive path for signals to connect layers disposed on opposing sides of the second layer 706,

such as a bottom layer to a top layer, and even a top surface and bottom surface of the second layer 706 itself. Additionally, the interconnect 702 may be extended through multiple layers, such as through a series of interconnects 702, a single multilayer interconnect 702, and the like.

[0051] EXEMPLARY EMBODIMENTS - METHODS

[0052] FIG. 8 is a flow chart depicting an embodiment of the present invention that illustrates an exemplary method 800 in which a signal is transmitted utilizing the interconnect 100. At block 802, a differential signal is transmitted through the interconnect 100 including the first conductor 104 and the second conductor 106. The differential signal may be provided to indicate a logical state, pass data, and the like. A first portion of the differential signal is transmitted through the first conductor 104 and a second portion of the differential signal is transmitted through the second conductor 106.

[0053] At block 804, EMI is encountered by the interconnect 100. For example, EMI may be transmitted through the semiconductor substrate 102 to the interconnect 100. The EMI may have a variety of sources, such as from power supplies, switching, and the like, as well as from a source that is outside a semiconductor device in a MEMS assembly employing the interconnect 100.

[0054] At block 806, the encountered EMI is distributed to the first conductor 104 and the second conductor 106. The EMI is distributed by the third conductor 110 so that the first conductor 104 and the second conductor 106 are symmetrically exposed. For instance, any EMI which is not shielded by the third conductor 110 from the first and conductors 104, 106 will be symmetrically distributed to the first and conductors 104, 106 so that substantially equivalent amounts of EMI are encountered. The substantially equivalent amounts of the symmetrically distributed EMI are incorporated into the differential signals being respectively transmitted through the first and second conductors 104 and 106.

[0055] At block 808, the EMI is removed from the differential signal. The EMI may be removed from the differential signal by referencing the first portion of the differential signal received from the first conductor 104 with the second portion of the differential signal received from the second conductor 106. For example, because the first portion and the second portion of the differential signal have

substantially equivalent amounts of the symmetrically distributed EMI, the EMI may be removed through common mode rejection. Thus, the differential signal that is transmitted through the interconnect 100 is substantially free of the EMI that was encountered by the third conductor 110.

[0056] It should be noted that in additional embodiments of the present invention, substantially equivalent amounts of EMI included in each of the first conductor 104 and the second conductor 106 may vary from one-to-one correspondence. For example, a designer of an embodiment of the present invention may configure the interconnect 100 to provide a desired signal-to-noise ratio to achieve desired functionality.

[0057] FIG. 9 is a flow chart depicting an embodiment of the present invention that illustrates an exemplary method 900 wherein an interconnect is produced. At block 902, a first conductor, a second conductor and a third conductor are formed from a semiconductor substrate. There are a variety of forming procedures that may be employed. For example, forming may include removing material from the semiconductor substrate so that the first conductor, second conductor and third conductor are defined in the semiconductor substrate. Material may be removed through steps which include etching (such as dry, wet, ion etching, etc., that results in isotropic and/or anisotropic etched surfaces) micro-machining, photolithography combined with etching, and the like.

[0058] An illustrative embodiment of the present invention is seen in Fig. 10, where a semiconductor device 1000 includes a semiconductor substrate 1002 having a first conductor 1004, a second conductor 1006, and a third conductor 1008. A first channel 1010 and a second channel 1012, formed by the removal of material from the semiconductor substrate 1002, define the first conductor 1004, the second conductor 1006 and the third conductor 1008 in the semiconductor substrate 1002.

[0059] The first conductor 1004, second conductor 1006, and third conductor 1008 which are used to form an interconnect may be disposed between opposing surfaces 1014, 1016 of the semiconductor substrate 1002. In one exemplary embodiment, the first, second and third conductors 1004, 1006, 1008 may be formed as generally perpendicular to a plane defined by the semiconductor

substrate 1002 of the semiconductor device 1000. This may be thought of as a vertical orientation, which shall be used to reference the orientation of the first, second and third conductors 1004, 1006, 1008 with respect to the semiconductor substrate 1002. Therefore, vertical orientation is not limited to general orientations in space. By defining the first, second and third conductors 1004, 1006, 1008 between the opposing surfaces 1014, 1016 of the semiconductor substrate 1002, signals may be passed through the semiconductor substrate 1002.

[0060] Referring again to method 900 in Fig. 9, an electrical insulator is formed at block 904. The insulator substantially surrounds the first conductor, the second conductor and the third conductor. The insulator may be formed in a variety of ways, such as through growing an oxide, depositing insulative material, and the like. As shown by an embodiment of the present invention in a semiconductor device 1100 depicted in FIG. 11, a first insulator 1102 and a second insulator 1104 fill the first channel 1010 and the second channel 1012 formed in the semiconductor substrate 1002 shown in FIG. 10.

[0061] FIG. 12 is an illustration of an embodiment of the present invention for the interconnect 1200 in which insulator is provided through multiple steps. When growing an oxide to provide an insulator as described previously respect to FIGS. 10-11, openings may be produced in which the oxide does not grow, such as a first opening 1202 and a second opening 1204. The first opening 1202 and the second opening 1204 may hinder structural integrity of the interconnect 1200, as well as the semiconductor substrate 1206 having the interconnect 1200. Therefore, the first opening 1202 and the second opening 1204 may be filled, such as with a structural material, to provide structure rigidity to the interconnect 1200. A variety of materials may be used as fill, such as polysilicon, and the like.

[0062] Although the invention has been described in language specific to structural features and methodological steps, it is to be understood that the invention defined in the appended claims is not necessarily limited to the specific features or steps described. Rather, the specific features and steps are disclosed as preferred forms of implementing the claimed invention.